Ramon Chips

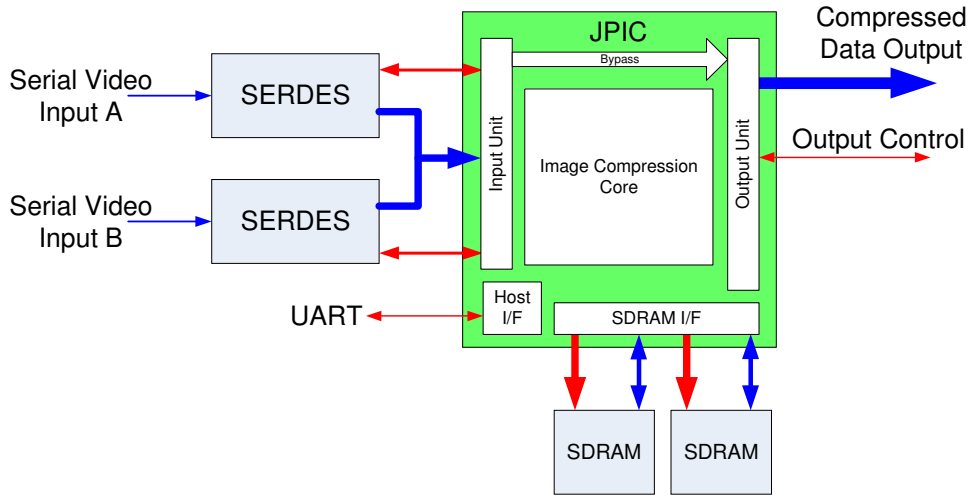
JPIC

- ✓ **JPEG 2000 encoder (compression)**
- ✓ **Requires two 256Mbit SDRAM chips**
- ✓ **Radiation hardened**
- ✓ **Input up to 12-bit pixels at 44 Mpixels/sec**
- ✓ **Two selectable input ports**
- ✓ **Output 24-bit compressed image data**
- ✓ **Output bursts at 44Mwords/sec enabling output multiplexing**
- ✓ **Low power dissipation**
- ✓ **Power down mode**

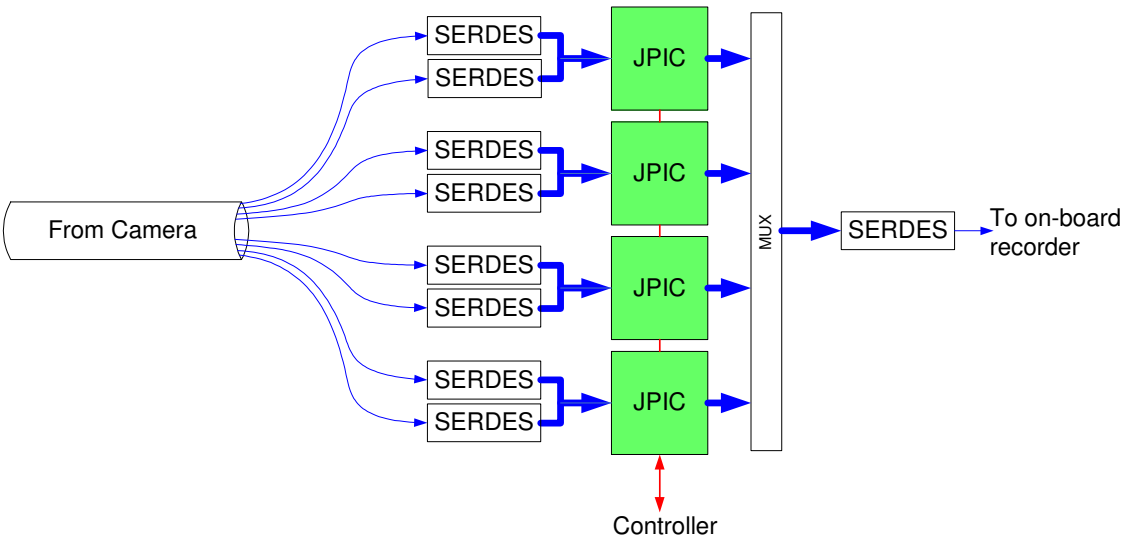
JPIC is a high-performance image compression ASIC that implements the JPEG2000 image compression standard. A modular architecture enables employing a single JPIC or multiple coordinated JPIC units. JPIC is designed to support any size of imager in optical, panchromatic and multi-spectral space and airborne sensors.

- Rad-Hard, provided as either Class Level S, Class Level B, or Ramon Chips' quality level RC1
- Radiation hardness:
  - TID: 300 Krad(Si)
  - SEL: LET > 106 Mev/cm2/mg
  - SEU: Cross section < 20µ2
  - EDAC protected on-chip memories
- 208pin QFP (ceramic hermetically sealed or plastic)
- Fabricated in 180nm CMOS
- 3.3V (I/O), 1.8V (core)
- 3 Watt in compression mode
- Contains 5Mbit on-chip memories and one million logic gates
- Input clock up to 44MHz, internally multiplied to 88MHz
- SDRAM interface up to 88MHz
- Controlled by a host via 1Mbaud UART chain link
- Multiple JPIC units can be controlled by a single host
- Programmable JPEG 2000 parameters, including compression rates, lossy / lossless compression, bypass without compression
- Enables system test with built-in synthetic image generation

The diagram demonstrates a typical JPIC system and the internal structure of the JPIC chip.



A typical system may combine multiple JPIC units and multiplex their outputs as they are transferred to storage.



CONTACT
Prof. Ran Ginosar, CEO
Phone +972-528-700-580, email ran@ramon-chips.com