RAMONchips

RC64 Many-Core DSP

64-Core High Performance Rad-Hard Single Chip Parallel DSP

Enabling Software Defined Satellites

Future constellations of communication, navigation and observation satellites will be software defined. Missions and capabilities will be flexibly redefined and upgraded while in orbit. To achieve this goal, super-computing is needed, mimicking today's clouds and virtualized data centers.

RC64, designed especially for software-defined satellites, is a many-core digital signal processor (DSP) enabling high performance computing in space. RC64 integrates sixty-four cores, 4MB shared memory and a dozen high-speed serial links, achieving 40 GFLOPS and up to 384 GOPS.

RC64 employs fine-grain parallelism, delivering linear scalability and near-linear speedup. Each 8/16/32-bit integer/floating-point DSP core provides 8-issue VLIW, up to 16-way SIMD and up to twenty operations per cycle.

RC64 on-chip 256-port shared memory enables direct access of each core. In addition, the cores contain a small private memory and write-through private instruction and data caches, eliminating coherency problems.

The 64 cores are managed at runtime by a hardware ***Synchronizer / Scheduler*** that automatically manages parallel tasks. It removes task management overhead from the cores and software, allocates tasks to the cores, enables nearly-perfect dynamic load balancing among the cores and facilitates task switching at a very high rate and very low latency. Allocated tasks are executed to completion before cores become available for new task allocation. Code and commands are downloaded into RC64 via two SpaceWire links or loaded from PROM.

A ***task-oriented programming model*** simplifies the conversion of serial code into parallel programs for RC64 and enables intuitive parallel programming of new applications by using standard C/C++ code and task graphs that indicate dependencies between tasks. A software development system for either Linux or Windows facilitates easy development, debugging, profiling and optimizing the code.

Samples of RC64 are planned for 2017. EM and early FM parts are due in 2018. Class S FM parts are expected in 2019.

Preliminary Specifications

- Fabricated on 65nm CMOS process
- Rad-hard RadSafe™ Ramon Chips technology
- Sixty-four 8/16/32-bit CEVA X1643 DSP cores
- Instruction cache, data cache and private memory per each core
- 300MHz clock frequency
- Each DSP core contains four flexible 32/16/8-bit MACs, total 76.8 (16-bit) GMAC/s
- VLIW cores enabling two load/store operations, two address modification operations, and up to 16 MAC operations, totaling 384 GOPS
- Sixty-four single-precision Floating Point Units
- Peak floating point performance 38.4 GFLOPS
- Modem (LDPC and Turbo-code) accelerators
- Hardware synchronizer/scheduler
- 4MB shared data memory
- DDR3 32-bit memory controller with 16-bit Reed-Solomon ECC at up to 800 MWord/s supporting up to 4 GByte memory
- NAND flash controller for boot and NVM storage with BCH page ECC
- Twelve high-speed serial links, 60 Gbit/sec I/O aggregate data rate, optimized for RC64-to-RC64 interconnect on same PCB and for board-to-board interconnect
- Serial Rapid IO and SpaceFibre protocols
- 48 LVDS links at 800 MWords/s for ADC/DAC
- Two SpaceWire links for code, commands and data download and for status and data upload
- Four SpaceWire links for instruments data and control
- Supports task-based parallel programming
- Power consumption: 1-10 Watts, depending on modes
- Package: 624 pins CCGA (optional PBGA)
- Temperature range –55ºC to +125ºC
- Temperature monitoring and stabilization
- Radiation hardness:
  - TID 300Krad(Si),
  - SEL LET > 106 Mev/cm^2/mg,
  - SEU rate < 1E-12 per bit-day,
  - EDAC protected on/off-chip memories
  - Detectors of SET, SEU and SEFI
  - Memory scrubbing
- MIL-STD-883 / MIL-PRF-385353 Class S, ESCC-9000

RC64 Applications

RC64 is easily programmable using task-oriented programming model.

- High performance space computing is enabled by using a single RC64 or by clustering multiple RC64 units on standard or customized boards and systems
- High speed inter-chip links enable smooth exchange of data among the multiple RC64 chips
- High capacity external DDR3 memories enable buffering and large data management
- High bandwidth communications to other on-board systems such as sensors, antennae and telecommunications is enabled by interfaces to multiple standard SERDES interfaces
- High bandwidth interfaces to ADC and DAC are designed to support high speed data I/O
- High speed SpaceWire links enable control & data interface to standard space computers and instruments

Software Development Tools

- Integrated development environment
  - Code editor
  - Compiler, assembler, linker
  - Many-core simulator
  - Many-core debugger
  - Many-core profiler
- Libraries
  - Libraries for frequently used functions
  - APIs for I/O configuration and control
  - APIs for host control and monitoring

Hardware Evaluation Platform

- 3U-VPX board, one RC64, ADC or DAC

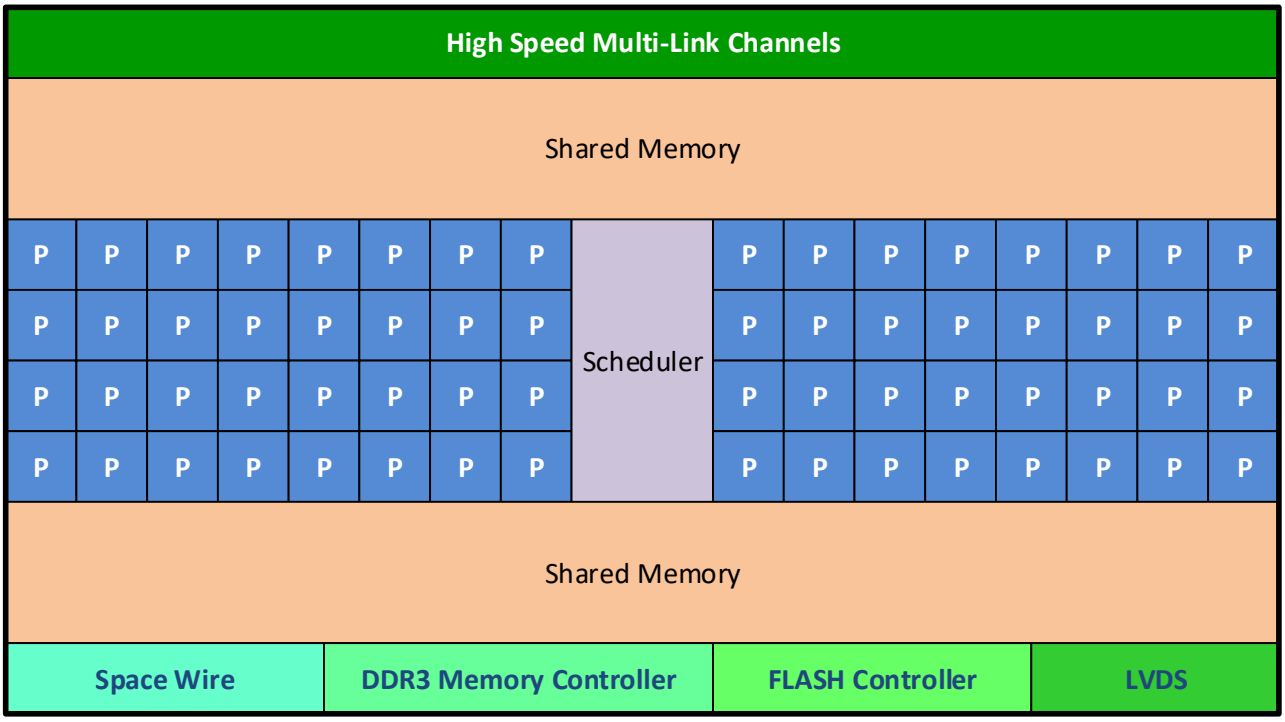
Sample Applications

Communication satellites

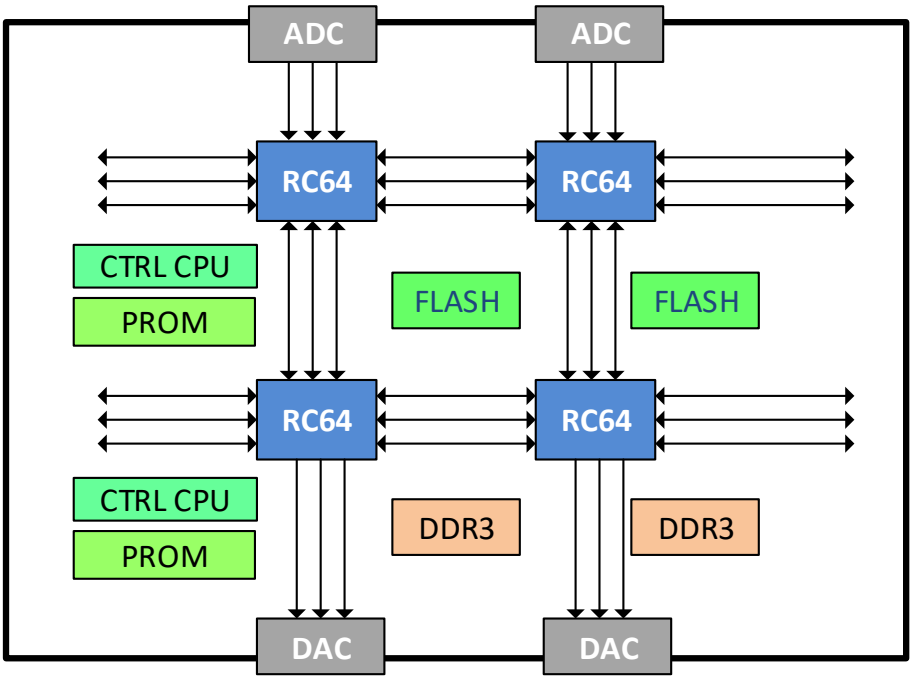
- Communication payload
- Digital/smart phased array antenna for communication and SAR satellites
- Flexible DVB-S2 and variations
- Communication jamming immunity
- Cyber protection
- Software defined radio
- IP routing in telecomm satellites
- Layers 4—7 network processing
- Deep packet inspection
- Transparent switching in telecomm satellites
- Regenerative switching in telecomm satellites
- Two-way high data rate flexible modems in telecomm satellites
- Digital beam forming
- Data modulation & encoding for telemetry

Earth observation, science and other satellites

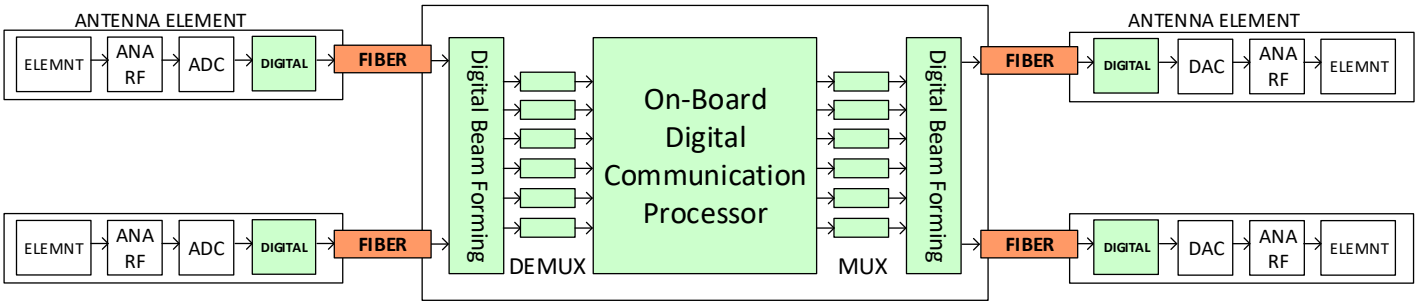
- Image compression in EOS
- Image processing in EOS
- Light stream image focusing
- Range processing
- Moving object identification
- Data exploitation
- Data fusion
- Signal transforms
- Back propagation algorithms
- Autonomous formation space flight
- Collision alert and avoidance
- Space situation awareness
- Navigation receivers & correlators
- In-orbit interference detection
- Inter-satellite orbit determination
- DDR3-based mass memory controller
- Cyber protection



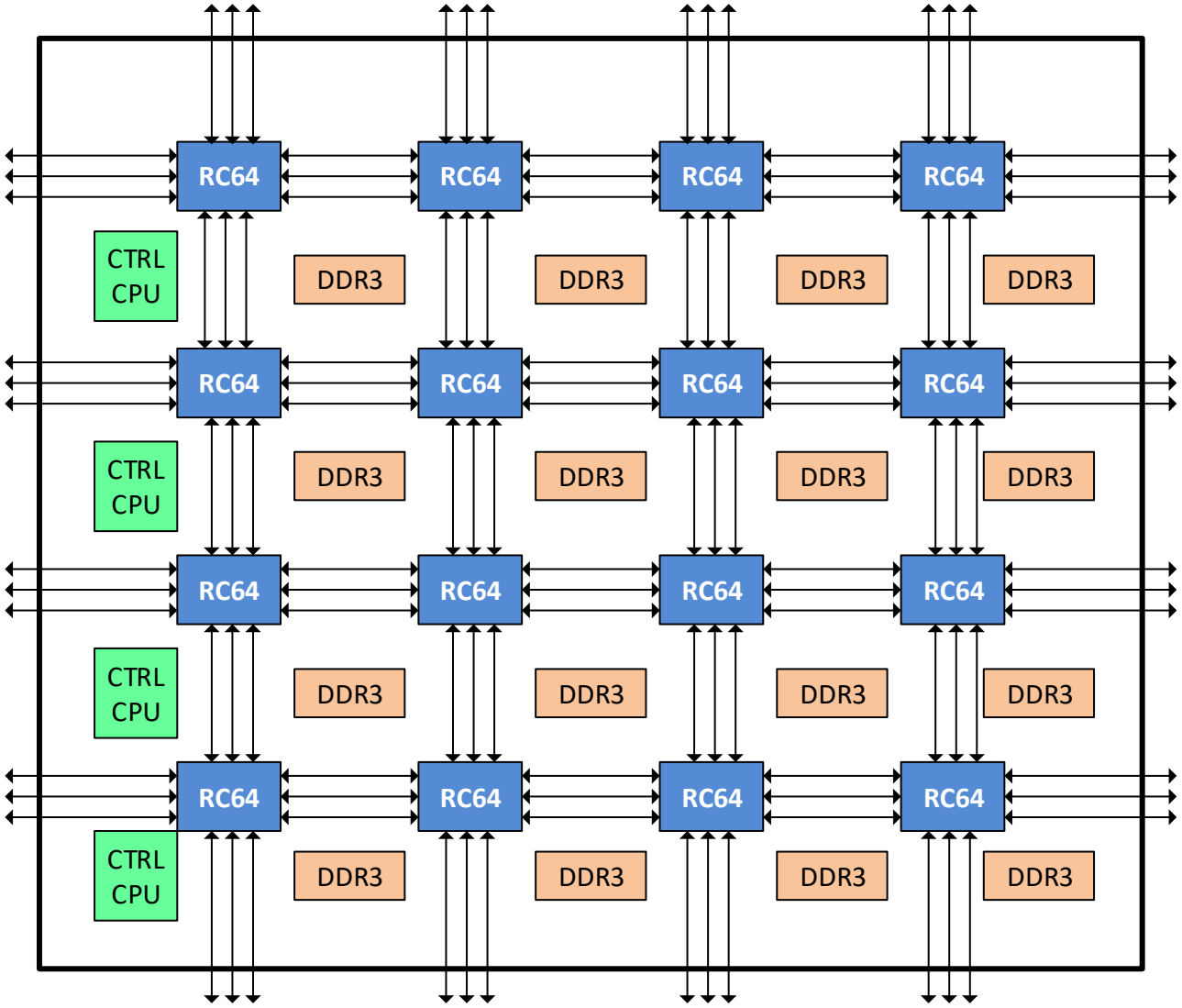
Rad-hard RC64 many-core architecture: 64 cores, scheduler, shared memory and rich interfaces



PCB Architecture with four RC64 chips and analog interfaces



Communication payload and digital phased array antenna using multiple RC64



High-performance Payload Computer, 16 high-speed interconnected RC64 units in a reprogrammable ensemble

Ramon Chips recommends its GR712RC dual-core rad-hard micro-processor for use as control CPU in RC64 systems.
GR712RC is available from Cobham Gaisler (www.gaisler.com)