RAMONchips

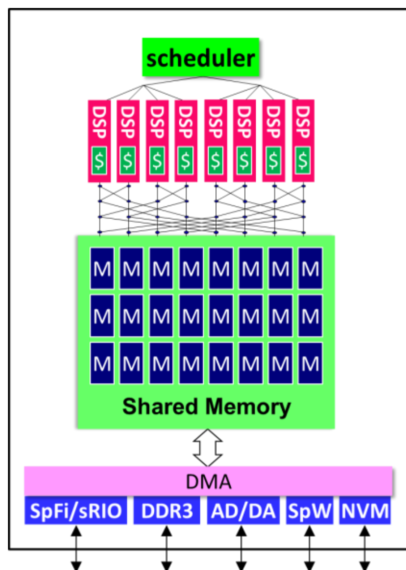
RC64 Many-Core DSP

64-Core High Performance Rad-Hard Single Chip Parallel DSP

Enabling Software Defined Satellites

Future constellations of communication, navigation and observation satellites will be software defined. Missions and capabilities will be flexibly redefined and upgraded while in orbit. To achieve this goal, super-computing is needed, mimicking today's clouds and virtualized data centers.

RC64, designed especially for software-defined satellites, is a many-core digital signal processor (DSP) and CPU enabling high performance computing in space. RC64 integrates sixty-four DSP/CPU cores, 4MB shared memory and a dozen high-speed serial links, achieving up to 38 GFLOPS and up to 150 GOPS.



RC64 employs fine-grain parallelism, delivering near-linear scalability and speedup. Each 8/16/32-bit integer/floating-point DSP core provides 8-issue VLIW, up to 16-way SIMD and up to twenty operations per cycle.

RC64 on-chip 256-port shared memory enables direct access of each core. In addition, the cores contain a small private memory and write-through private instruction and data caches, eliminating coherency problems.

The 64 cores are managed at runtime by a hardware ***Synchronizer / Scheduler*** that automatically manages parallel tasks. It removes task management overhead from the cores and software, allocates tasks to the cores, enables nearly-perfect dynamic load balancing among the cores and facilitates task switching at a very high rate and very low latency. Allocated tasks are executed to completion before cores become available for new task allocation. Code and commands are downloaded into RC64 via two SpaceWire links or uploaded from PROM.

A ***task-oriented programming model*** simplifies the conversion of serial code into parallel programs for RC64 and enables intuitive parallel programming of new applications by using standard C/C++ code and task graphs that indicate dependencies between tasks. A software development system for either Linux or Windows facilitates easy development, debugging, profiling and optimizing the code.

Samples of RC64 are available. EM and early FM parts are due in 2018.

Sample Applications

Communication satellites

- Communication payload
- Flexible DVB-S2 and variations
- Communication jamming immunity
- Cyber protection, Encryption and authorization
- Software defined radio
- IP routing in telecomm satellites
- Layers 4—7 network processing
- Deep packet inspection
- Transparent switching in telecomm satellites
- Regenerative switching in telecomm satellites
- Digital beam forming and Smart Antennas
- Data modulation & encoding for telemetry
- Digital/active phased array antenna elements for communication and SAR satellites
- Machine learning and neural networks

Earth observation, science and other satellites

- Image compression in EOS
- Image processing in EOS
- Light stream image focusing
- Range processing
- Moving object identification
- Data exploitation
- Data fusion
- Signal transforms
- Back propagation algorithms
- Autonomous formation space flight
- Collision alert and avoidance
- Space situation awareness
- Navigation receivers & correlators
- In-orbit interference detection
- Inter-satellite orbit determination
- DDR3-based mass memory controller
- Cyber protection
- Encryption and authorization

Ramon Chips, an Israeli privately held, government-funded enterprise making chips and systems for space, has made JPIC (an image compression IC employed in earth observation missions) and GR712RC, a rad-hard dual-core LEON3 space processor employed in multiple missions in earth orbits and deep space. GR712RC is marketed globally by Cobham Gaisler.

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Preliminary Specifications

- Fabricated on 65nm CMOS process
- Rad-hard RadSafe™ Ramon Chips technology
- Sixty-four 8/16/32-bit CEVA X1643 DSP/CPU cores
- Instruction cache, data cache and private memory per each core
- Thirty-two IO/DMA and special function controllers
- 200 MHz clock frequency
- Each DSP/CPU core contains four flexible 32/16/8-bit MACs, achieving 50 (16-bit) GMAC/s
- VLIW cores enable two load/store operations, two address modification operations, and up to four MAC operations per cycle
- Peak 16-bit fixed-point multiply and add performance 100 GOPS
- Sixty-four single-precision Floating Point Units
- Peak single-precision floating point performance 25 GFLOPS
- Modem FEC accelerator for LDPC and Turbo-code
- Hardware synchronizer / scheduler
- 4MB 256-ported shared memory
- DDR3 (optionally DDR2) 32-bit memory controller with 16-bit Reed-Solomon ECC at 600 MWord/s supporting up to 4 GByte off-chip DDR3 memory
- NAND flash controller for boot and NVM storage with BCH page ECC
- 12 high-speed serial links, 60 Gbit/sec input and 60 Gbit/sec output aggregate data rate
- SpaceFibre and Serial Rapid IO protocols
- 48 LVDS links at 800 MWords/s for ADC/DAC
- Two SpaceWire links for code, commands and data download and for status and data upload
- Four SpaceWire links for instrument data
- Supports task-based parallel programming
- Power consumption: 1-10 Watts, depending on modes
- Package: 665 pins PBGA
- Temperature range: –55ºC to +125ºC
- Temperature monitoring and stabilization
- Space qualified to Ramon Chips Class RC2
- Radiation hardness:
    - TID 300Krad(Si)
    - SEL LET > 106 Mev·cm^2/mg
    - SEU rate < 10^{-12} errors per bit-day
    - EDAC protected on/off-chip memories
    - Detectors of SET, SEU and SEFI
    - Memory scrubbing

Software Development Tools

- Integrated development environment
    - Code editor
    - Compiler, assembler, linker
    - Many-core simulator
    - Many-core debugger
    - Many-core profiler
- Libraries
    - Libraries for frequently used functions
    - APIs for I/O configuration and control
    - APIs for host control and monitoring
    - Software for high reliability and FDIR

Hardware Evaluation Platform

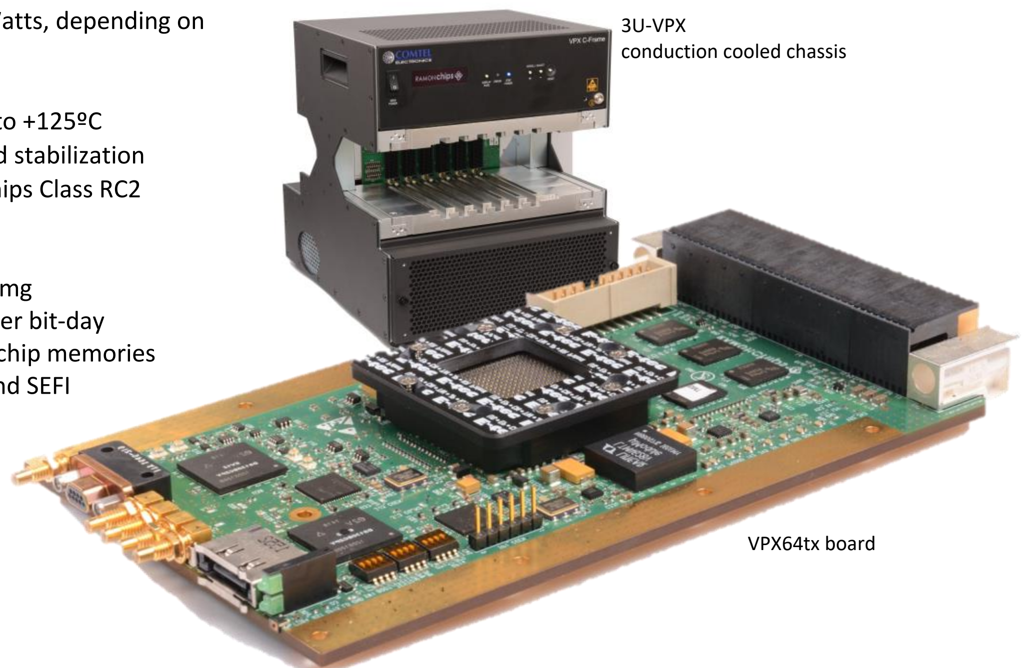
- VPX64 – 3U-VPX, RC64, DDR3 and Flash
- VPX64tx – VPX64 with two DACs
- VPX64rx – VPX64 with two ADCs
- 3U-VPX conduction-cooled chassis

ROADMAP

Class S qualification (MIL-STD-883, MIL-PRF-38535 and ESCC9000) may be applied, including conversion to CCGA package.

Flip-chip PBGA with top-level heat removal may be manufactured for alternative PCB formats and alternative methods of heat dissipation.

Future silicon versions of the manycore will exploit advanced technologies to enhance performance by integrating many more cores, larger memory and faster I/O and to achieve higher performance-to-power ratio.



3U-VPX conduction cooled chassis

VPX64tx board

All specifications subject to change without notice © 2017 Ramon Chips, Ltd.